Amendments to the Specification

Please amend the following paragraphs/sections as indicated.

Please amend the paragraph starting on page 4, line 2, as follows:

The present invention provides alignment and ordering of vector elements for SIMD processing. The present invention is implemented in a computer system including a processor having a plurality of registers. ~~In the~~ In one embodiment, in the generation of an aligned vector of first width from two second width vectors ~~alignment of vector elements~~ for SIMD processing, one vector is loaded from a memory unit into a first register and another vector is loaded from the memory unit into a second register. The first vector contains a first byte of ~~an~~ the aligned vector to be generated. Then, a starting byte specifying the first byte of ~~an~~ the aligned vector is determined. Next, ~~a~~ the aligned vector is extracted from the first register and the second register beginning from the first bit in the ~~first~~ starting byte of the first register continuing through the bits in the second register. Finally, the ~~extracted~~ aligned vector is replicated into a third register such that the third register contains a plurality of elements aligned for SIMD processing. ~~In the ordering of vector elements for SIMD processing, a first vector is loaded from a memory unit into a first register and a second vector is loaded from the memory unit into a second register. Then, a subset of elements is selected from the first register and the second register. The elements from the subset are then replicated into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.~~

Please add the following paragraphs after the paragraph starting on page 4, line 2, as follows (with no underlining):

In another embodiment, an aligned vector is generated from two source vectors for SIMD processing. In this embodiment, a first source vector is loaded into a first register, and a second source vector is loaded into a second register. Then, a first plurality of elements is read from the first register and a second plurality of elements is read from the second register. Finally, the first plurality of elements and the second plurality of elements are written into a third register in a particular order to produce a target vector having a plurality of elements aligned for SIMD processing. In one embodiment, the writing step includes writing even-numbered, lower elements of the first register to the third register and writing sign bits of odd-numbered, lower elements of the first register to the third register. In another embodiment, the writing step includes writing even-numbered, upper elements of the first register to the third register and writing sign bits of odd-numbered, upper elements of the first register to the third register.

In another embodiment, an ordered set of elements in a target vector are generated from elements in a first source vector and a second source vector for SIMD processing. In this embodiment, the first source vector is loaded into a first register and a second source vector is loaded into a second register. Then, a first subset of elements is selected from the first register. The first subset includes any one of the following groups of elements from the first source vector: odd elements, even elements, lower elements, and upper elements. Finally, a second subset of elements is selected from the second register. The second subset includes any one of the following groups of elements from the second source vector: odd elements, even elements, lower elements, and upper elements. One embodiment also

includes the step of writing the first and second subsets of elements into a third register to facilitate a particular SIMD vector processing operation. In this embodiment, the first subset is written into any one of the following groups of elements in the third register: upper elements, odd elements, and odd elements in reverse order. Also in this embodiment, the second subset is written into any one of the following groups of elements in the third register: lower elements, even elements, and even elements in reverse order. Elements written into the third register comprise the target vector.

Please amend the Abstract, starting on page 42, line 2, as follows:

The present invention provides alignment and ordering of vector elements for SIMD processing. In the generation of an aligned vector of first width from two second width vectors, ~~alignment of vector elements for SIMD processing,~~ one vector is loaded from a memory unit into a first register and another vector is loaded from the memory unit into a second register. The first vector contains a first byte of ~~an~~ the aligned vector to be generated. Then, a starting byte specifying the first byte of ~~an~~ the aligned vector is determined. Next, ~~a~~ the aligned vector is extracted from the first register and the second register beginning from the first bit in the ~~first~~ starting byte of the first register continuing through the bits in the second register. Finally, the ~~extracted~~ aligned vector is replicated into a third register such that the third register contains a plurality of elements aligned for SIMD processing. ~~In the ordering of vector elements for SIMD processing, a first vector is loaded from a memory unit into a first register and a second vector is loaded from the memory unit into a second register. Then, a subset of elements are selected from the first register and the second register. The elements from the subset are then replicated into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.~~